WHAT IS CLAIMED IS:

1. A synchronous semiconductor memory device comprising:

a data output circuit adapted to generate data output up and down signals and to perform a data output operation synchronously to an external clock in response to the data output up and down signals; and

an on-die termination (ODT) circuit adapted to generate ODT up and down signals for performing an ODT operation, said ODT up and down signals having a same timing as the data output up and down signals.

2. The device as claimed in 1, wherein the data output circuit comprises:

a data output multiplexer adapted to multiplexing read data applied through a data path by using the first and second clock signals, to generate the data output up and down signals; and

an output driver adapted to perform the data output operation synchronized to the external clock, the output driver comprising,

a pull-up driver, and

a pull-down driver,

wherein the output driver controls an on operation and an off operation of the pull-up driver and the pull-down driver in response to a state of the data output up and down signals.

3. The device as claimed in 1, wherein the ODT circuit comprises:

an ODT synchronous buffer adapted to receive an ODT command applied in response to a buffered clock signal generated by buffering the external clock, and outputting a synchronous ODT command in response to a first clock signal delay-locked to the external clock;

an ODT gate adapted to pass through and latch the synchronous ODT command in response to the first clock signal and a second clock signal that has a fixed phase difference with respect to the first clock signal, to generate the ODT up and down signals; and

an ODT driver adapted to perform an ODT driving operation synchronized to the external clock, by controlling an on operation and an off operation of a pull-up resistance and a pull-down resistance in response to a state of the ODT up and down signals.

4. The device as claimed in 3, further comprising a delay-locked loop adapted to generate the first clock signal delay-locked to the external clock.

5. The device as claimed in 3, wherein the phase difference between the first and second clock signals is based on a half cycle of the external clock.

6. The device as claimed in 3, wherein the ODT synchronous buffer comprises:

a delay adapted to delay the ODT command for a fixed time;

a first flip-flop adapted to latch an output of the delay in response to the buffered clock signal, to determine a set-up time and a hold time of the ODT command; and

a second flip-flop adapted to latch an output of the first flip-flop in response to the first clock signal, to generate the synchronous ODT command.

7. The device as claimed in 6, wherein the ODT gate comprises:

a first inverter adapted to invert a level of the synchronous ODT command;

a first transmission gate adapted to transmit an output of the first inverter in response to the first clock signal having a first state;

a first latch adapted to latch an output of the first transmission gate;

a second transmission gate adapted to transmit an output of the first latch in response to the second clock signal having a first state;

a second latch adapted to latch an output of the second transmission gate to generate the ODT down signal;

a P-type MOS transistor having a gate connected to an output of the first transmission gate, a source connected to a

power voltage, and a drain connected to an output terminal of the second transmission gate; and

a second inverter adapted to invert an output of the second latch to generate the ODT up signal.

8. The device as claimed in 7, wherein the ODT driver comprises:

an output pad; and

a plurality of unit drivers, wherein each of said unit drivers comprises,

a pull-up resistance having a first end directly connected to a common node,

a pull-down resistance having a first end directly connected to the common node,

a pull-up transistor having a drain connected to a second end of the pull-up resistance, a source connected to the power voltage, and a gate adapted to respond to the ODT up signal when the unit driver is enabled by an up enable signal, and

a pull-down transistor having a drain connected to second end of the pull-down resistance, a source connected to a ground voltage, and a gate adapted to respond to the ODT down signal when the unit driver is enabled by a down enable signal,

wherein the common node of each of the unit drivers is connected to the output pad.

9. The device as claimed in 8, wherein the data output circuit includes an output driver having a same configuration as the ODT driver, except that the pull-up resistors and pull-down resistors of the ODT driver are replaced by straight through connections in the output driver.

10. A synchronous semiconductor memory device comprising:

a data output circuit adapted to generate data output up and down signals and to perform a double data rate (DDR) data output operation synchronously to an external clock in response to the data output up and down signals; and

an on-die termination (ODT) circuit adapted to generate ODT up and down signals for performing an ODT operation, said ODT up and down signals having a same timing as the data output up and down signals.

11. The device as claimed in 10, wherein the ODT circuit comprises:

an ODT synchronous buffer adapted to receive an ODT command applied in response to a buffered clock signal generated by buffering the external clock, and outputting a synchronous ODT command in response to a first clock signal delay-locked to the external clock;

an ODT gate adapted to pass through and latch the synchronous ODT command in response to the first clock signal and a second clock signal that has a fixed phase difference with respect to the first clock signal, to generate the ODT up

and down signals;

an ODT controller adapted to output an up enable signal and a down enable signal in response to an external or internal control; and

an ODT driver adapted to control an on operation and an off operation of a pull-up resistance and a pull-down resistance, in response to a state of a combined up signal obtained by logically combining a state of the ODT up signal and a state of the up enable signal and a state of a combined down signal obtained by logically combining a state of the ODT down signal and a state of the down enable signal, to perform an ODT driving operation synchronized to the external clock.

12. The device as claimed in 11, wherein the data output circuit comprises:

a data output multiplexer adapted to multiplexing memory cell data applied through a data path by using the first and second clock signals, to generate the data output up and down signals; and

an output driver adapted to perform the data output operation synchronized to the external clock, the output driver comprising,

a pull-up driver, and

a pull-down driver,

wherein the output driver controls an on operation and an off operation of the pull-up driver and the pull-down driver in response to a state of the data output up and down

signals.

13. The device as claimed in 12, wherein the phase difference between the first clock signal and the second clock signal is based on a half cycle of the external clock.

14. The device as claimed in 11, further comprising a delay-locked loop adapted to generate the first clock signal delay-locked to the external clock.

15. The device as claimed in 11, wherein the ODT synchronous buffer comprises:

a delay adapted to delay the ODT command for a fixed time;

a first flip-flop adapted to latch an output of the delay in response to the buffered clock signal, to determine a set-up time and a hold time of the ODT command; and

a second flip-flop adapted to latch an output of the first flip-flop in response to the first clock signal, to generate the synchronous ODT command.

16. The device as claimed in 15, wherein the ODT gate comprises:

a first inverter adapted to invert a level of the synchronous ODT command;

a first transmission gate adapted to transmit an output of the first inverter in response to the first clock signal

having a first state;

a first latch adapted to latch an output of the first transmission gate;

a second transmission gate adapted to transmit an output of the first latch in response to the second clock signal having a first state;

a second latch adapted to latch an output of the second transmission gate to generate the ODT down signal;

a P-type MOS transistor having a gate connected to an output of the first transmission gate, a source connected to a power voltage, and a drain connected to an output terminal of the second transmission gate; and

a second inverter adapted to invert an output of the second latch to generate the ODT up signal.

17. The device as claimed in 16, wherein the ODT driver comprises:

an output pad; and

a plurality of unit drivers, wherein each of said unit drivers comprises,

a gating part adapted to receive the ODT up and down signals and the up and down enable signals, to logically combine the ODT up signal and the up enable signal to produce the combined up signal, and to logically combine the ODT down signal and the down enable signal to produce the combined down signal,

a pull-up resistance having a first end directly

connected to a common node,

a pull-down resistance having a first end directly connected to the common node,

a pull-up transistor having a drain connected to a second end of the pull-up resistance, a source connected to the power voltage, and a gate adapted to receive the combined up signal, and

a pull-down transistor having a drain connected to second end of the pull-down resistance, a source connected to a ground voltage, and a gate adapted to receive the combined down signal,

wherein the common node of each of the unit drivers is connected to the output pad.

18. The device as claimed in 17, wherein the data output circuit includes an output driver having a same configuration as the ODT driver, except that the pull-up resistors and pull-down resistors of the ODT driver are replaced by straight through connections in the output driver.

19. The device as claimed in 17, wherein, when the ODT controller outputs the up and down enable signals in response to an external control, a mode register set code is externally received.

20. The device as claimed in 17, wherein the ODT controller includes a fuse for generating an internal, control

signal.

21. The device as claimed in 17, wherein some among the plurality of unit drivers are enabled only when an ODT resistance value is 75 ohms.

22. The device as claimed in 17, wherein the plurality of unit drivers each have different pull-up and pull-down resistance values.

23. An on-die termination (ODT) method in a synchronous semiconductor memory device having a data output circuit for performing a data output operation synchronously to an external clock, said method comprising:

generating data up and down signals for the data output operation;

generating ODT up and down signals having a same timing as the data output up and down signals for the data output operation; and

performing an ODT operation corresponding to a state of the ODT up and down signals when an ODT command is applied to control pull-up and pull-down resistances within ODT drivers.